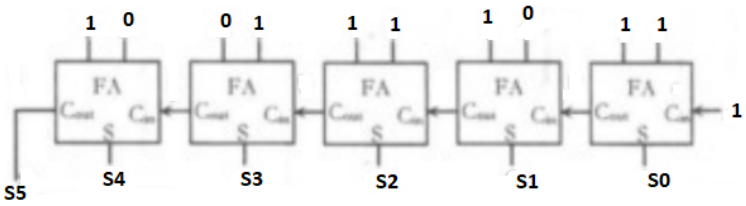
Started on Sunday, 15 August 2021, 3:00 PM
State Finished
Completed on Sunday, 15 August 2021, 4:02 PM
Time taken 1 hour 2 mins
Grade **21.88** out of 25.00 (**88**%)

Question 1
Complete
Mark 1.25 out of 1.25

What is the output for the following circuit:



a. 000101
b. 001001
c. 100101
d. 110101
e. 101001

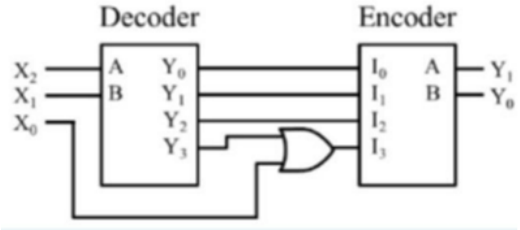
The correct answer is:
100101

Question **2**

Complete

Mark 1.25 out of 1.25

Assume that I0 has the lowest priority, show the output Y1Y0 for X2X1X0= 111



a. None is correct

b. 10

c. 11

d. 00

e. 01

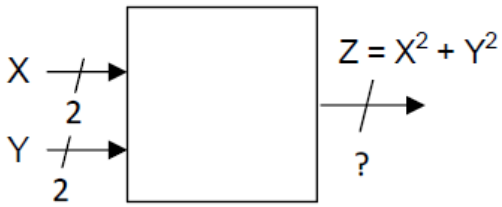
The correct answer is:
11

Question **3**

Complete

Mark 1.25 out of 1.25

The circuit has two inputs X and Y each is a 2-bit unsigned umber. It has an output number Z such that



the minimum number of bits required for the output number Z is

Select one:

a. 4

b. 5

c. 3

d. 2

The correct answer is: 5

Question 4

Complete

Mark 0.63 out of 1.25

A demultiplexer is used to ...

- a. None is correct
- b. Perform serial to parallel conversion
- c. Route the data from single input to one of many outputs
- d. All is correct
- e. Select data from several inputs and route it to single output

The correct answers are:
Route the data from single input to one of many outputs,
Perform serial to parallel conversion

Question 5

Complete

Mark 1.25 out of 1.25

You asked to design a combinational logic circuit which takes a 4-bit unsigned number X (X_3 X_2 X_1 X_0) as input and produces an output F which equals the result of integer division of X by 3 (e.g., if X=7, F=2). How many bits does the output F have?

Select one:

- a. 4 bits
- b. 3 bits
- c. 1 bit
- d. 2 bits

The correct answer is: 3 bits

Question 6

Complete

Mark 1.25 out of 1.25

The size of the smallest multiplexer that can be used to implement any function of the form F(A,B,C,D) without any other logic gates (not even invertor) is:

- a. 8x1
- b. 32x1
- c. 2x1
- d. 16x1
- e. 4x1

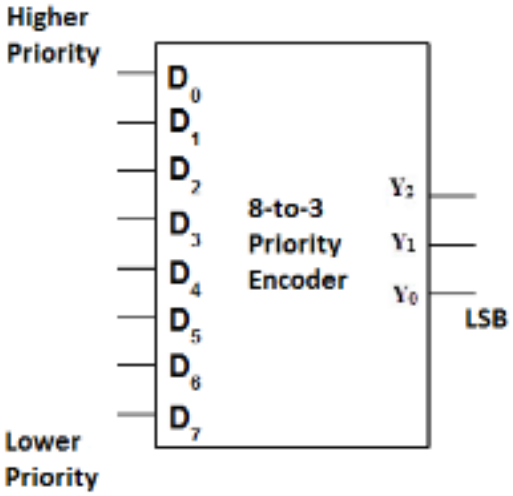
The correct answer is:
16x1

Question 7

Complete

Mark 1.25 out of 1.25

In the priority encoder shown below. D_0 is highest priority and D_7 is the lowest priority, the output $Y_2Y_1Y_0 = 101$ when the status at inputs D_0-D_7 is as described in _____with all other inputs being in a don't care condition.



Select one:

- a. $D_1 = 1$ and $D_2 = 1$.
- b. $D_3 = 1$ and $D_5 = 1$.
- c. $D_0 = 1$ and $D_2 = 1$.
- d. $D_6 = 1$ and $D_5 = 1$.

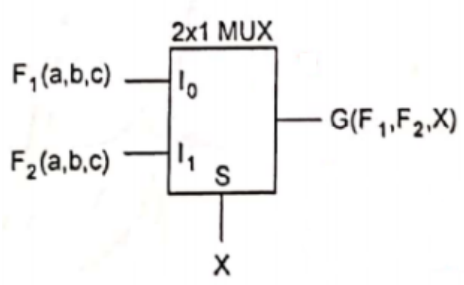
The correct answer is: $D_6 = 1$ and $D_5 = 1$.

Question 8

Complete

Mark 1.25 out of 1.25

Having the following diagram, represent the function G in terms of F1(a,b,c) , F2(a,b,c) and X.



Select one:

- a. X` F1 + X F2
- b. X` F1 + X F2`
- c. X` F1 + F2
- d. X F1 + X` F2
- e. X` F1` + X F2

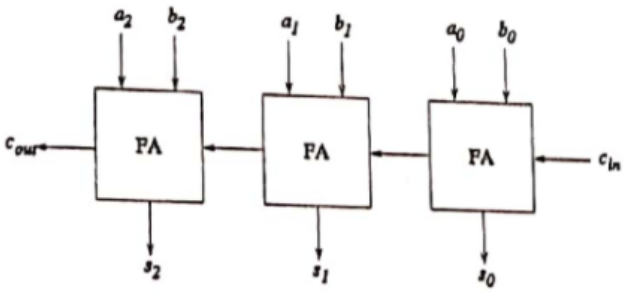
The correct answer is: X` F1 + X F2

Question 9

Complete

Mark 1.25 out of 1.25

Consider the following diagram of a 3-bit adder:



What is the value of s2, s1, s0 and Cout, if a2a1a0 = 101 and b2b1b0= 110 and Cin =0 ?

Select one:

- a. s2 s1s0 = 011 and Cout= 1
- b. s2 s1s0 = 001 and Cout= 1
- c. s2 s1s0 = 011 and Cout= 0
- d. s2 s1s0 = 0110 and Cout= 1
- e. s2 s1s0 = 010 and Cout= 1

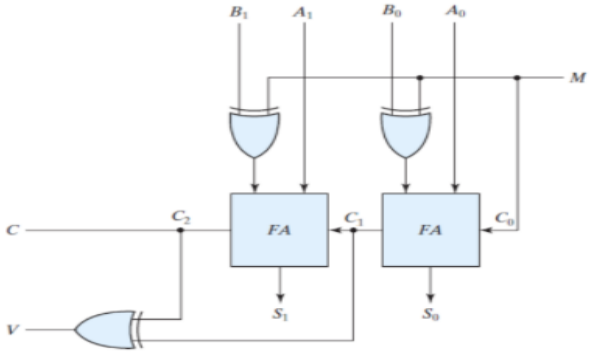
The correct answer is: s2 s1s0 = 011 and Cout= 1

Question **10**

Complete

Mark 0.00 out of 1.25

For the following two-bit adder/subtractor with overflow detection. If inputs **M=0**, two unsigned numbers **A1A0= 01**, **B1B0= 01**, what's the value of **S1**, **S0**, **C**, and **V**?



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a. **S1 S0** = 11, **C**= 1, **V**= 0

b. **S1 S0** = 10, **C**= 1, **V**= 1

c. **S1 S0** = 10, **C**= 1, **V**= 0

d. **S1 S0** = 10, **C**= 0, **V**= 0

e. **S1 S0** = 01, **C**= 1, **V**= 0

The correct answer is:
S1 S0 = 10, **C**= 1, **V**= 0

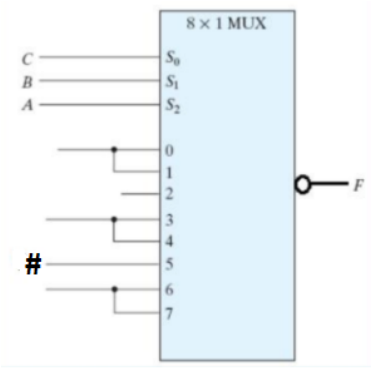
Question 11

Complete

Mark 0.00 out of 1.25

The circuit below implements the following function using a MUX, what should be the input labeled (**#**) connected to?

F(A,B,C,D)= **∑(1, 3, 4, 11, 12, 13, 14, 15)**



a. 1

b. 0

c. D

d. D`

The correct answer is:
D

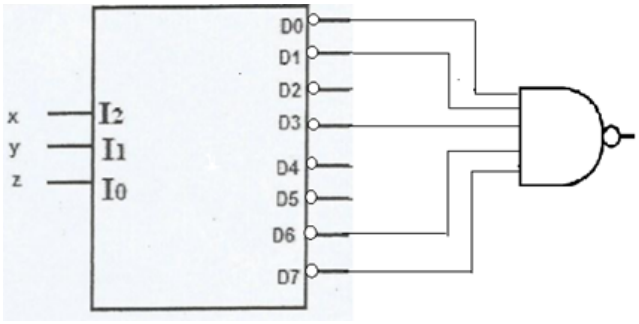
Question 12

Complete

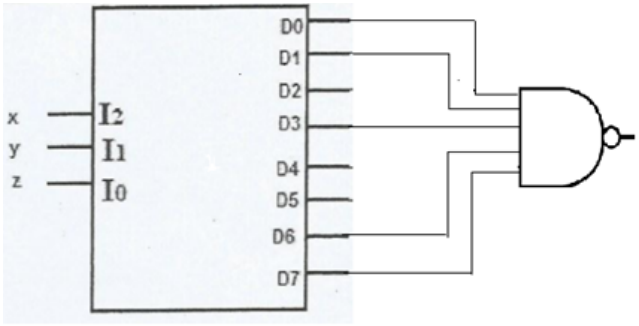
Mark 1.25 out of 1.25

The correct Implementation of f(x,y,z) = ∏ (2,4,5) using 3x8 Decoder and one NAND gate

a.

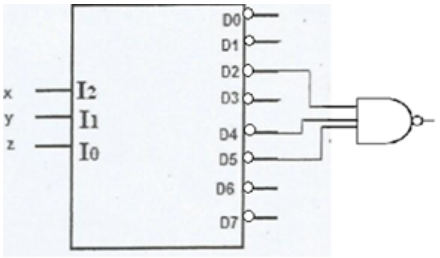


b.

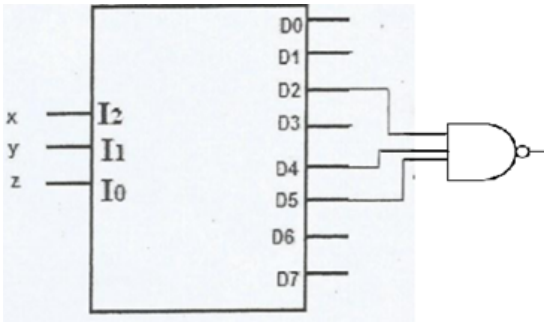


c. None is correct

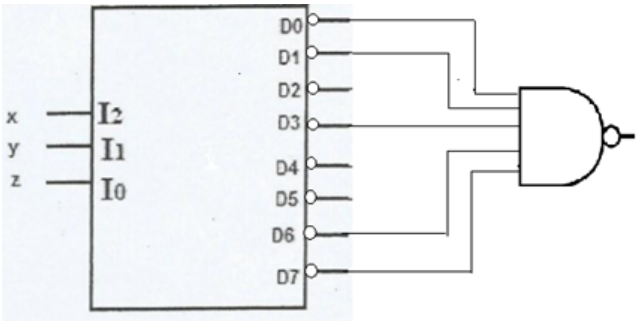
d.



e.



The correct answer is:

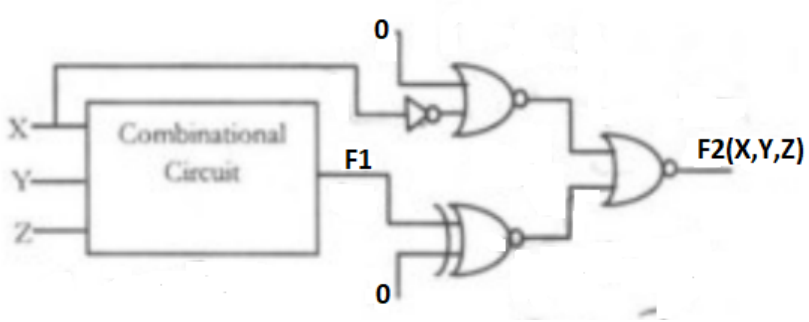


Question 13

Complete

Mark 1.25 out of 1.25

Write the reduced Boolean expression for **F1(X,Y,Z)**, Given that **F2(X,Y,Z)= X`YZ**



- a. YZ
- b. Y`Z`
- c. Y`+Z`
- d. XY
- e. Y+Z

The correct answer is:
YZ

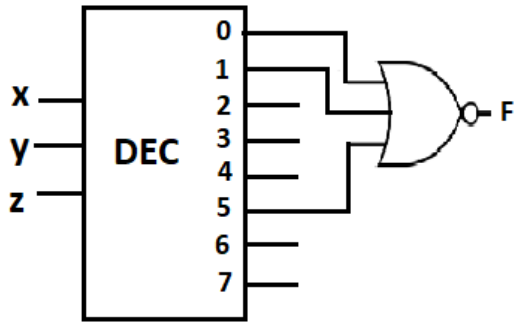
Question 14

Complete

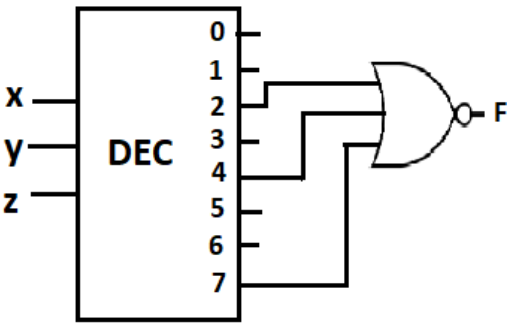
Mark 1.25 out of 1.25

Implement F(x,y,z)= Σ(2,3,4,6,7) using Decoder and one NOR gate

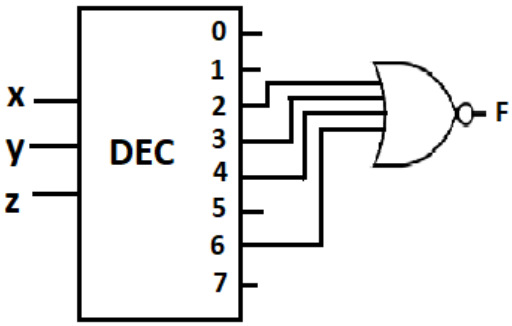
a.



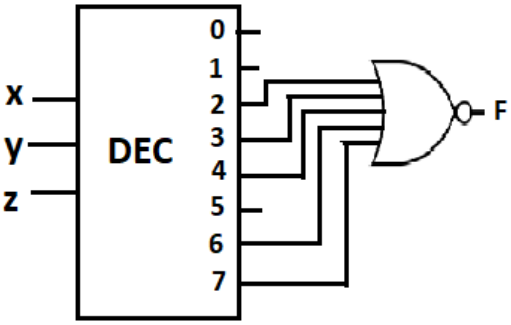
b.



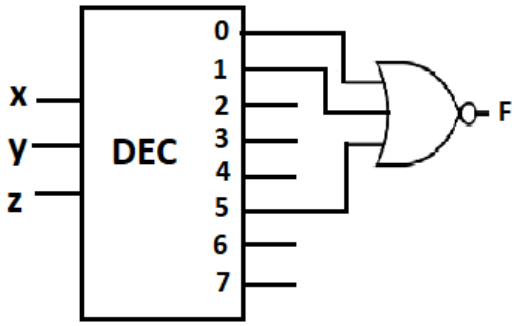
c.



d.



The correct answer is:



Question **15**

Complete

Mark 1.25 out of 1.25

The following is a Verilog behavioral description for the module *CKT*.

The *CKT* is a _____.

```
module CKT(I, Y, X);
    input [1:0] I;
    input X;
    output [0:3] Y;
    reg [0:3] Y;
    always @(I or X)
        case ({X, I})
            3'b000: Y = 4'b1000;
            3'b001: Y = 4'b0100;
            3'b010: Y = 4'b0010;
            3'b011: Y = 4'b0001;
            default:Y = 4'b1000;
        endcase
endmodule
```

Select one:

- a. 2-to-4 decoder with enable active high enable
- b. 2-to-4 decoder with enable active low enable
- c. 4-to-16 decoder with enable active high enable
- d. 4-to-16 decoder with enable active low enable
- e. 4-to-1 Mux with enable active high enable

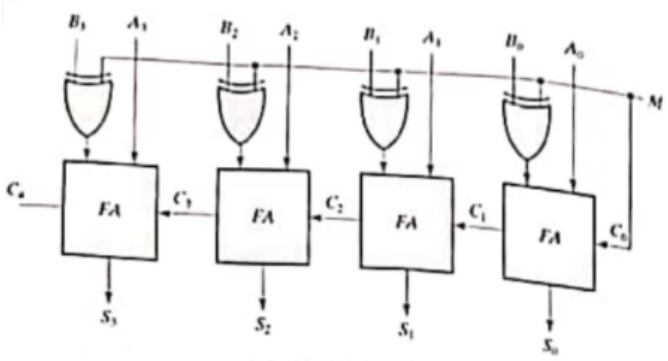
The correct answer is: 2-to-4 decoder with enable active low enable

Question 16

Complete

Mark 1.25 out of 1.25

Consider the following diagram of a 4-bit adder/ subtractor:



Configure the value of M, A3, A2, A1, A0 the above circuit to implement 4-bit 2's complement, such that the input is B3 B2 B1 B0, and the output S3 S2 S1 S0= **(2's of (B3 B2 B1 B0))**

a. **M=1, A3=1, A2=1, A1=1, A0=1**

b. **M=0, A3=0, A2=0, A1=0, A0=0**

c. **M=1, A3=0, A2=0, A1=0, A0=0**

d. **M=0, A3=1, A2=1, A1=1, A0=1**

The correct answer is:
M=1, A3=0, A2=0, A1=0, A0=0

Question 17

Complete

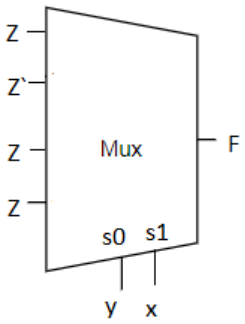
Mark 1.25 out of 1.25

Implement the following function using **only one 4-to-1 MUX without enable**, no other gates allowed (But invertors are allowed).

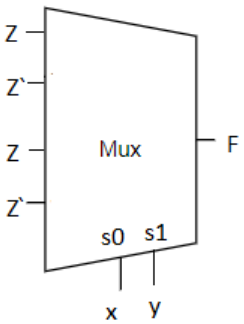
f(x,y,z)= x ⊕ y ⊕ z

Select one:

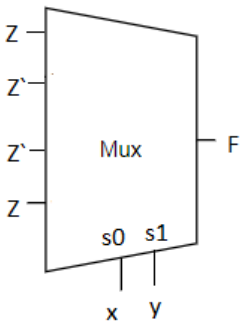
a.



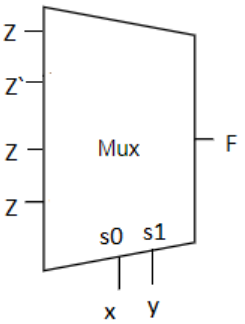
b.



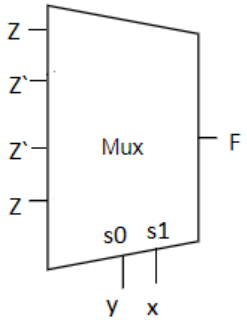
c.



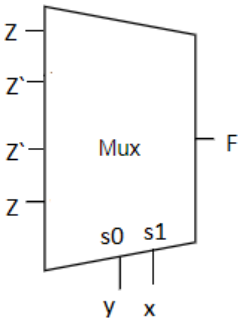
d.



e.



The correct answer is:

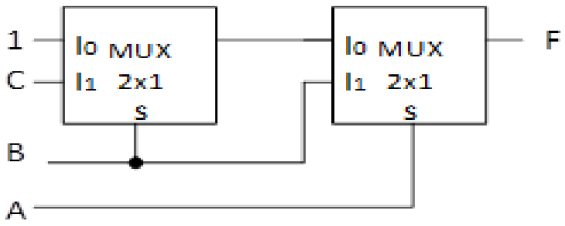


Question **18**

Complete

Mark 1.25 out of 1.25

The circuit represents the Boolean function



a. $F(A.B.C) = A'C + A'B'$

b. $F(A,B,C) = ABC + A'B'$

c. $F(A,B,C) = AB + A'C + A'B'$

d. None

e. $F(A,B,C) = AB + A'C$

The correct answer is:

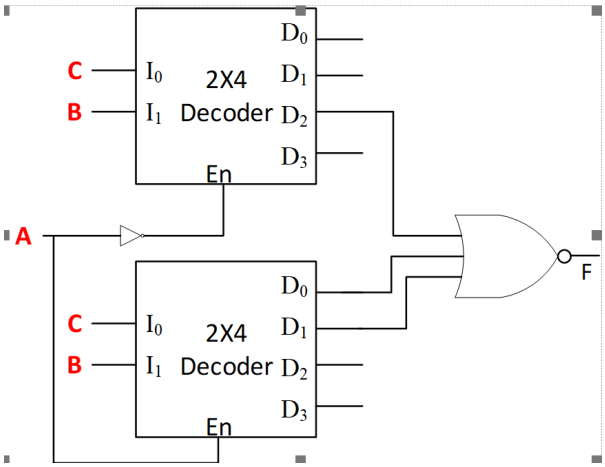
$F(A,B,C) = AB + A'C + A'B'$

Question 19

Complete

Mark 1.25 out of 1.25

The function F(A,B,C) of this implemented circuit is:



a. None

b. F = ∑(1, 3, 6, 7)

c. F = ∑(0, 1, 3, 6, 7)

d. F = ∑(0, 1, 6, 7)

e. F = ∑(0, 1, 3, 6)

The correct answer is:
F = ∑(0, 1, 3, 6, 7)

Question 20

Complete

Mark 1.25 out of 1.25

The largest decoder we can build using five 2-to-4 decoders with Enable *without* any additional components is a

Select one:

a. 4-to-16 decoder

b. 3-to-8 decoder

c. 6-to-64 decoder

d. 5-to-32 decoder

The correct answer is: 4-to-16 decoder

◄ First Exam

Jump to...

Final Exam (All Sections) ►